TECH PUBLIC
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TPAX810MS3

Microprocessor Reset Circuit

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FEATURES

- High Accurate ±2%
- Precision monitoring of +3V, +3.3V, and +5V Power supply voltage
- Fully specified over temperature
- Available in three output configurations
- Push-Pull (RESET) high output (TPAX810)
- 200ms typ. Power-on reset pulse width
- 25μs supply current
- Guaranteed reset valid to V_{CC}=+1V
- Power supply transient immunity

APPLICATION

- Battery-operated systems and controllers
- Intelligent instruments
- Critical μP and μC power monitoring
- Portable / Battery powered equipment
- Automotive

The TPAX810 series are used for microprocessor (μP) supervisory circuits to monitor the power supplies in μP and digital systems. They provide excellent circuit reliability and low cost by eliminating external components and adjustments when used with +5V, +3.3V, +3.0V, +2.5V powered circuits.

These circuits perform a single function: they assert a reset signal whenever the V_{CC} supply voltage declines below a preset threshold, keeping it asserted for at least 200ms after V_{CC} has risen above the reset threshold. Reset thresholds suitable for operation with a variety of supply voltages are available. TPAX810 series have push pull outputs. TPAX810 series has an active low RESET output, while the TPAX810 has an active high RESET output The reset comparator is designed to ignore fast transients on V_{CC}, and the outputs are guaranteed to be in the correct logic state for V_{CC} down to 1.0V. Low supply current makes TPAX810 series ideal for use in portable equipment.

Ordering Information

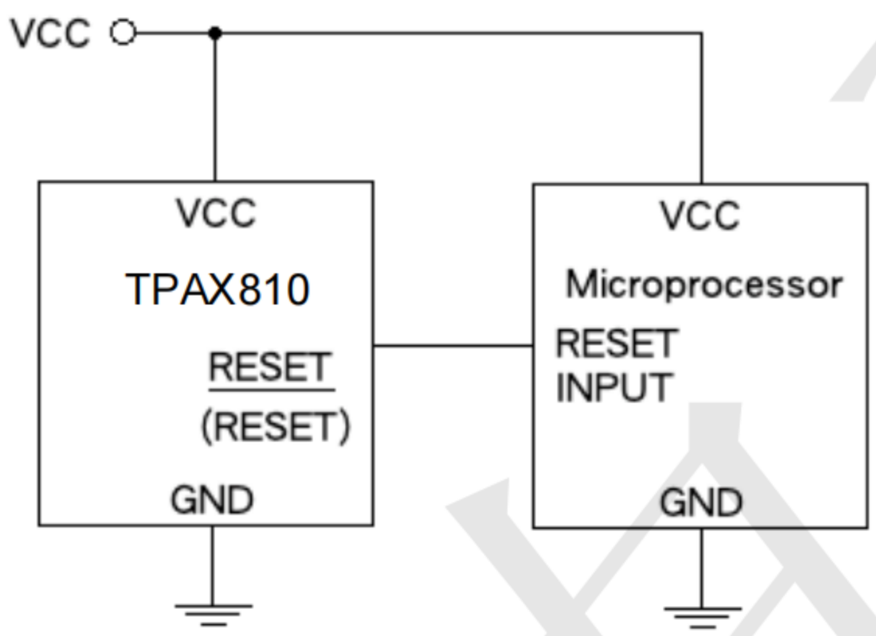
TPAX 810 MS3

RESET VOLTAGE: L=4.63V
M=4.38V
T=3.08V
S=2.93V
R=2.63V

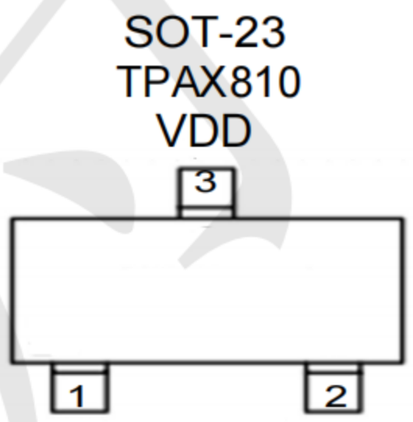
Marking:

TPAX810LS3: AGAA
TPAX810MS3: AHAA
TPAX810TS3: AJAA
TPAX810SS3: AKAA
TPAX810RS3: ALAA

TYPICAL APPLICATIN CIRCUIT



Pin Definition



GND	(RESET)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	LIMIT	UNIT
Terminal Voltage (with respect to GND)	V_{CC}	GND - 0.3 to GND +6.5	V
RESET & (RESET) push-pull	V_{RESET}	GND - 0.3 to V_{CC} +0.3	V
Input Current, V_{CC}	I_{CC}	20	mA
Output Current, RESET, (RESET)	I_O	5	mA
Power Dissipation	P_D	$(T_J-T_A)/R_{\theta JA}$	mW
Operating Junction Temperature Range	$T_{J.OPR}$	-40 ~ +125	°C
Storage Temperature Range	T_{STG}	-65 ~ +150	°C
Lead Soldering Temperature (260°C)	T_{LEAD}	10	s

THERMAL PERFORMANCE

PARAMETER	SYMBOL	MAXIMUM	UNIT
Thermal Resistance from Junction to Case	$R_{\theta JC}$	110	°C/W
Thermal Resistance from Junction to Ambient (Note 1)	$R_{\theta JA}$	250	°C/W

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C unless otherwise noted)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Input Supply Voltage	T_A=-40°C~+85°C	V_{CC}	1.0	--	6	V
Supply Current	V_{CC}=V_{TH} + 1V	I_{CC}	--	25	35	μA
Reset Threshold	TPAX810L	V_{TH}	4.54	4.63	4.71	V
	TPAX810M		4.29	4.38	4.46	
	TPAX810T		3.02	3.08	3.15	
	TPAX810S		2.87	2.93	3.00	
	TPAX810R		2.57	2.63	2.69	
Reset Threshold Temperature Coefficient	T_A=0~+85ºC	V_{THT}	--	50	--	ppm/°C
Set-up Time	V_{CC} = 0 ~ (V_{TH} - 100mV)	T_{SET}	1	--	--	μs
V_{CC} to Reset Delay	V_{CC} = V_{TH} ~ (V_{TH} - 100mV)	T_{RD}	--	20	--	μs
Reset Active Timeout Period	T_A=0~+85ºC	T_{DELAY}	140	200	260	ms
RESET Output (MAX809) Voltage Low	1.8V<V_{CC}<$V_{TH(MAX)}$, I_{SINK} =1.2mA	V_{OL}	--	--	0.3	V
	1.2V<V_{CC}<1.8V, I_{SINK} =50μA					
RESET Output (MAX809) Voltage High	V_{CC} > $V_{TH(MAX)}$, I_{SOURCE} =500μA	V_{OH}	0.8 V_{CC}	--	--	V
(RESET) Output (MAX810) Voltage Low	V_{CC} > $V_{TH(MAX)}$, I_{SINK} =1.2mA	V_{OL}	--	--	0.3	V

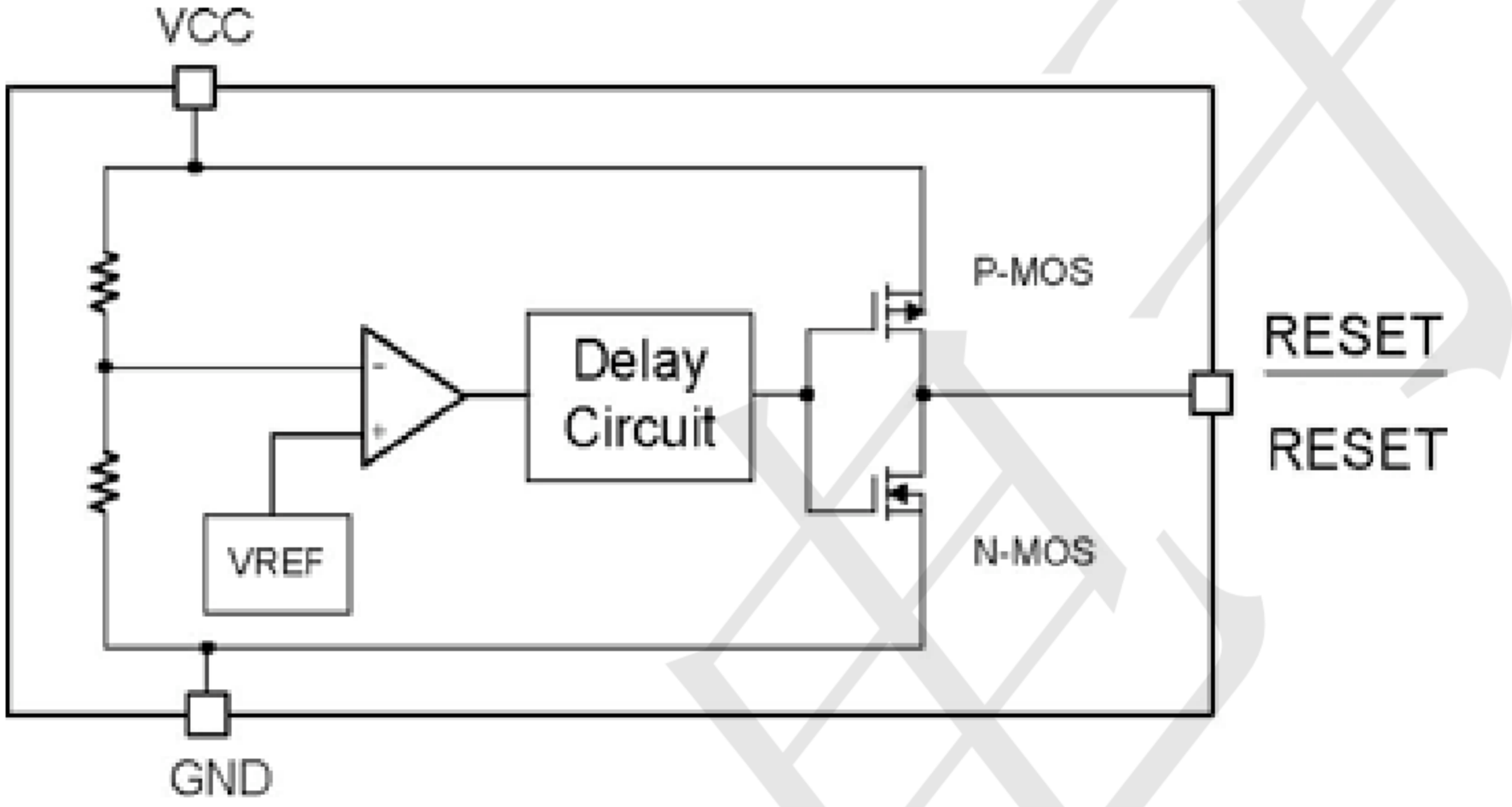
ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C unless otherwise noted)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
(RESET) Output (MAX810) Voltage High	1.8V<V_{CC}<$V_{TH(MAX)}$, I_{SOURCE} =500μA	V_{OH}	0.8 V_{CC}	--	--	V
	1.2V<V_{CC}<1.8V, I_{SOURCE} =150μA					
Hysteresis at V_{CC}	Input Voltage	V_{HVS}	--	40	--	mV

Note :

1. $R_{\theta JA}$ is measured the PCB copper area of approximately 1in^2 (Multi-layer). Needs to connect to V_{SS} pin.

BLOCK DIAGRAM



APPLICATION INFORMATION

Negative-Going V_{CC} transients in addition to issuing a reset to the µP during power-up, power-down, and brownout conditions, the TPAX810 are relatively immune t o short-duration negative-going V_{CC} transients (glitches).
The TPAX810 does not generate a reset pulse. The graph was generated using a negative going pulse applied to V_{CC}, starting 0.5V above the actual reset threshold and ending below it by the magnitude indicated (reset comparator overdrive). The graph indicates the maximum pulse width a negative going V_{CC} transient can have without causing a reset pulse. As the magnitude of the transient increases (goes farther below the reset threshold), the maximum allowable pulse width decreases. Typically, a V_{CC} transient that goes 100mV below the reset threshold and lasts 20µS or less will not cause a reset pulse. A 0.1µF bypass capacitor mounted as close as possible to the V_{CC} pin provides additional transient immunity.

FUNCTION DESCRIPTION

A microprocessor's reset input starts the µP in a known state. The TPAX810 assert reset to prevent code-execution errors during power-up, power-down, or brownout conditions. They assert a reset signal whenever the V_{CC} supply voltage declines below a preset threshold, keeping it asserted for at least 140ms after V_{CC} has risen above the reset threshold. The TPAX810 have a push-pull output stage.

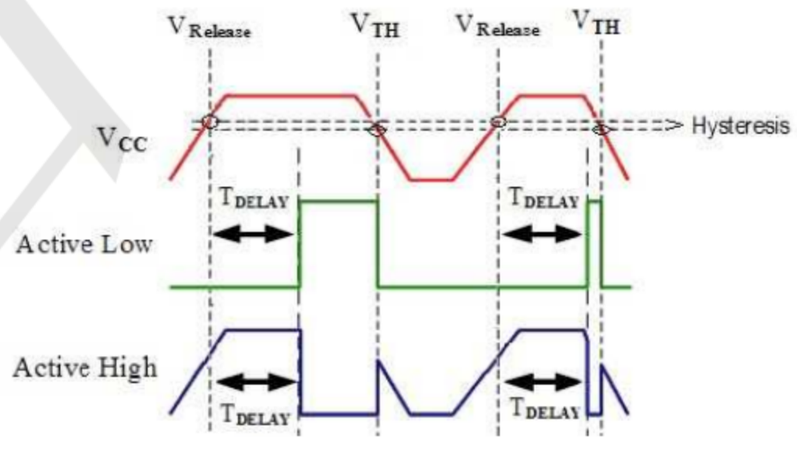
ENSURING A VALID RESET OUTPUT DOWN TO V_{CC}=0

RESET is guaranteed to be a logic low for V_{CC} > 1.0V. Once V_{CC} exceeds the reset threshold, an internal timer keeps RESET low for the reset timeout period; after this interval, RESET goes high. If a brownout condition occurs (V_{CC} dips below the reset threshold), RESET goes low. Any time V_{CC} goes below the reset threshold, the internal timer resets to zero, and RESET goes low. The internal timer starts after V_{CC} returns above the reset threshold, and RESET remains low for the reset timeout period. When V_{CC} falls below 1V, the TPAX810 reset output no longer sinks current - it becomes an open circuit. Therefore, high impedance CMOS logic input connected to reset can drift to undetermined voltages. This present no problem in most applications since most µP and other circuitry is inoperative with V_{CC} below 1V.However, in applications where reset must be valid down to 0V, adding a pull down resistor to reset causes and stray leakage currents to flow to ground, holding reset low (Figure 2.) R1's value is not critical; 100K is large enough not to load reset and small enough to pull RESET to ground. For the TPAX 810 if reset is required to remain valid for V_{CC} <1V.

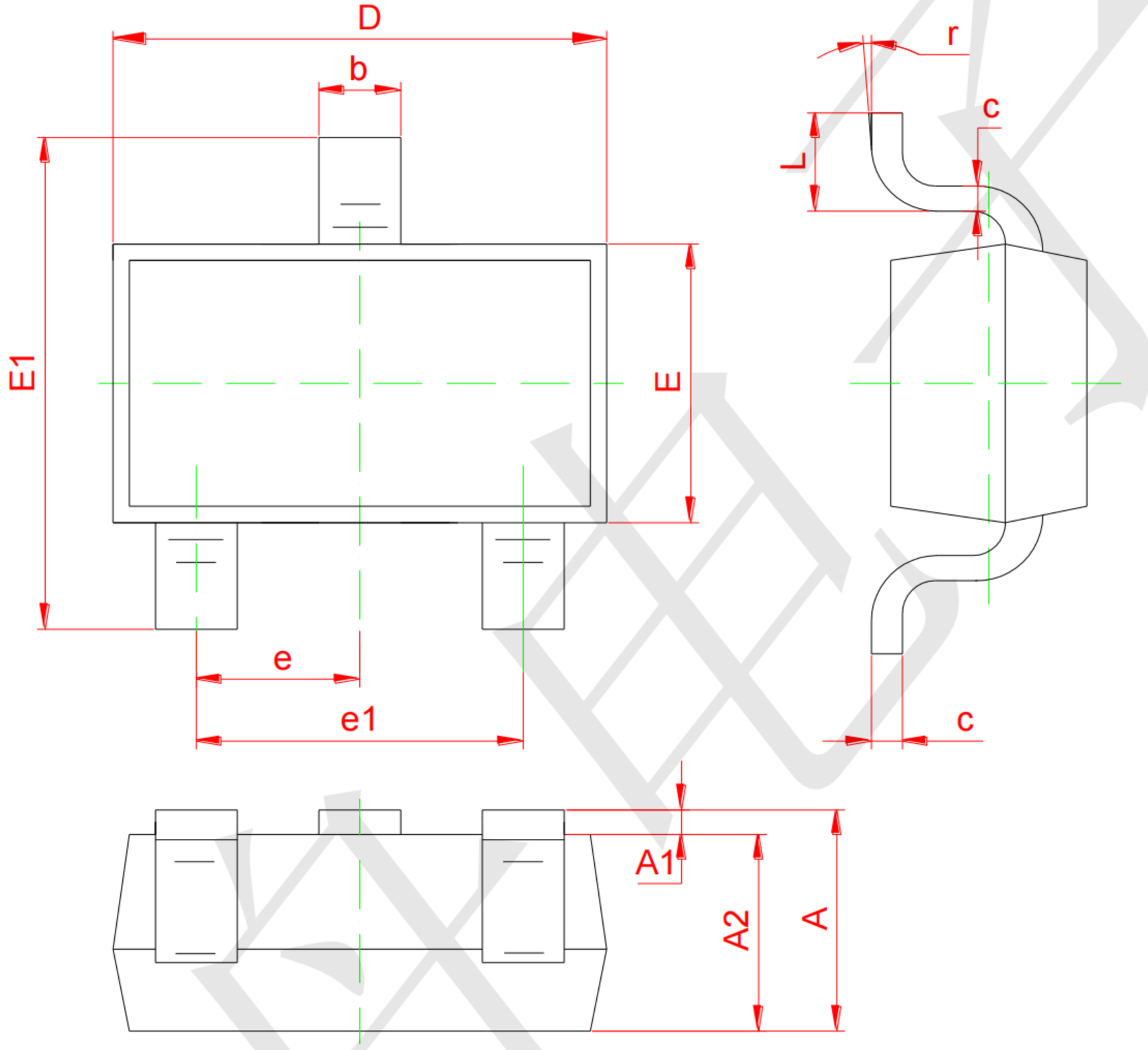
BENEFITS OF HIGHLY ACCURATE RESET THRESHOLD

Most µP supervisor ICs has reset threshold voltages between 5% and 10% below the value of nominal supply voltages. This ensures a reset will not occur within 5% of the nominal supply, but will occur when the supply is 10% below nominal. When using ICs rated at only the nominal supply ±5%, this leaves a zone of uncertainty where the supply is between 5% and 10% low, and where the reset many or may not be asserted.

TIMMING DIAGRAM



Package informantion



Symbol	Dimensions In Millimeters	
	Min	Max
A1	0.02	0.1
A2	1.0Typical	
b	0.4Typical	
c	0.1Typical	
D	2.70	3.10
E	1.10	1.50
E1	2.20	2.60
e1	1.80	2.00
L	0.35	0.48