TP6328GS6

600kHz 18V 3A Synchronous COT Step-Down Converter

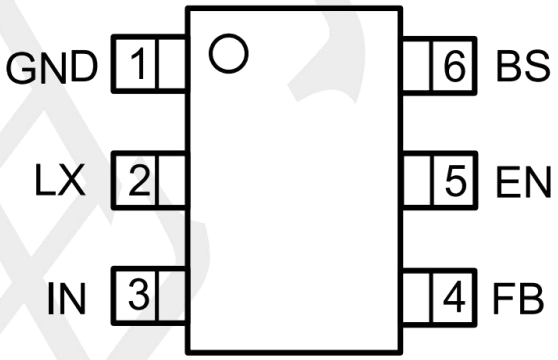
Features

- 70mΩ/35mΩ Low $R_{DS(ON)}$ internal FETs
- High Efficiency Synchronous-Mode Operation
- Wide Input Range:4.5V to 18V
- Output Voltage from 0.765V
- 600kHz Switch Frequency
- Up to 3A, 3.5A@1.2V Output Current
- COT control to achieve fast transient responses
- Power Save Mode at Light Load
- Integrated internal compensation
- Stable with Low ESR Ceramic Output Capacitors
- Over Current Protection with Hiccup Mode
- Thermal Shutdown
- Inrush Current Limit and Soft Start
- Build in Input Over Voltage Protection
- Compact package: SOT23-6

Applications

- Flat Panel Television and Monitors
- Digital Set Top Boxes
- Wireless and DSL Modems
- Notebook computer

Pinout (top view)



Pin Configurations

Pin Number	Pin Name	Pin Function
1	GND	Ground pin.
2	LX	Switching Pin.
3	IN	Power supply Pin
4	FB	Output Voltage feedback input. Connect FB to the center point of the external resistor divider.
5	EN	Drive this pin to a logic-high to enable the IC. Drive to a logic-low to disable the IC and enter micro-power shutdown mode. Don't floating EN.
6	BS	Bootstrap. A capacitor connected between LX and BS pins is required to form a floating supply across the high-side switch driver.

Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
VIN	Input Supply Voltage, EN	-0.3	20	V
LX	LX voltage range	-0.3	20	
	LX Voltages (<10ns transient)	-4.5	22	
FB	FB, pin voltage range	-0.3	6	
BS	BS, pin voltage range	-0.3	26	
	BS to LX Voltage	-0.3	6	
PD	PD @ TA = 25°C	1		W
LT	Lead Temperature (Soldering, 10 sec.)	260		℃
Temperature	Junction Temperature (Note2)	160		
	Storage, Tstg	-65	150	

ESD Rating

Items	Description	Value	Unit
V_{ESD_HBM}	Human Body Model for all pins	±2000	V
V_{ESD_CDM}	Charged Device Model for all pins	±1000	V

JEDEC specification JS-001

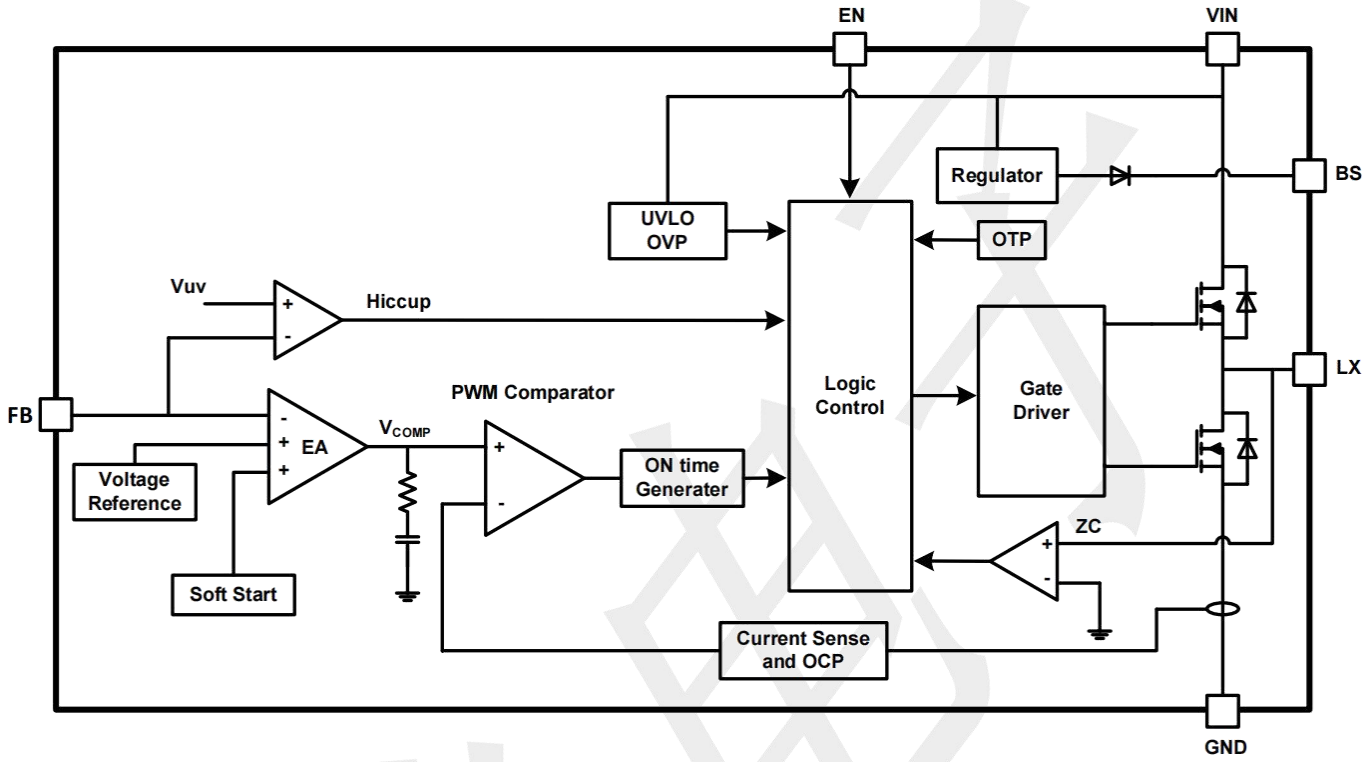
Recommended Operating Conditions

Items	Description	Min	Max	Unit
Voltage Range	IN	4.5	18	V
T_J	Operating Junction Temperature	-40	125	°C

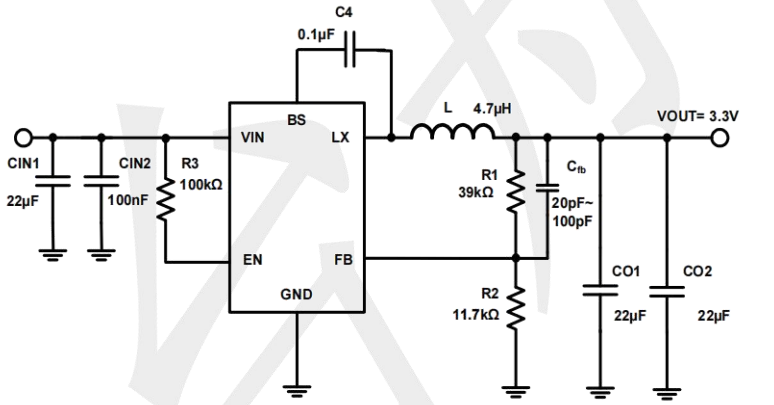
Thermal Resistance (Note3)

Items	Description	Value	Unit
θ_{JA}	Junction-to-ambient thermal resistance	100	°C/W
θ_{JC}	Junction-to-case(top) thermal resistance	56	°C/W
θ_{JB}	Junction-to-board thermal resistance	16.2	°C/W
ψ_{JC}	Junction-to-case(top) characterization parameter	2.0	°C/W

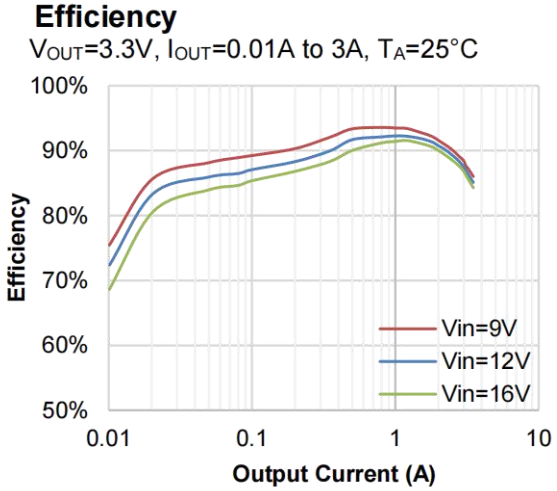
BLOCK DIAGRAM



Typical Application Circuit



Typical Application Circuits (V_{REF}=0.765V)



Electrical Characteristics

(VIN = 12V, VOUT = 3.3V, TA = 25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST Conditions	MIN	TYP	MAX	UNIT
Supply Voltage	V_{IN}		4.5	--	18	V
OVP Threshold	OVP		18.7	19.3	19.8	V
UVLO Rising Threshold	UVLO		--	4.3	--	V
UVLO Hysteresis	UVLO		--	0.35	--	V
Quiescent Current	I_Q	V_{EN}=2V,V_{FB}=V_{REF}X105%	--	300	--	uA
Shutdown Current	I_{SHDN}	EN=0, V_{IN}=12V	--	5	10	uA
Feedback Reference Voltage	V_{REF}	TA = 25°C	0.75	0.765	0.78	V
Top FET RON	$R_{DS(ON)1}$		--	70	--	mΩ
Bottom FET RON	$R_{DS(ON)2}$		--	35	--	mΩ
Switch Valley Current Limit	I_{LIM}	Minimum Duty Cycle	3.7	4.0	4.5	A
High-Side Switch Leakage Current		V_{IN}= 0V, V_{LX}=0V	1	--	10	uA
EN Rising Threshold			0.85	0.95	1.05	V
EN Hysteresis			--	180	--	mV
Maximum Duty Cycle			--	90	--	%
Switching Frequency	F_{SW}	Maximum Duty Cycle	450	600	750	KHz
Minimum On-Time(Note 4)			--	80	--	uS
Soft-start Time	t_{SS}		0.5	0.8	1.2	mS
Hiccup on Time(Note 4)			--	1.2	--	mS
Hiccup Time Before Restart(Note 4)			--	3.6	--	mS
Thermal Shutdown Threshold(Note 4)	T_{SD}		--	165	--	℃
Thermal Shutdown Hysteresis(Note 4)	T_{HYS}		--	30	--	℃

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.
Note 2: TJ is calculated from the ambient temperature TA and power dissipation PD according to the following formula: $T_J = T_A + P_D \times \theta_{JA}$. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_{D\,(MAX)} = (T_{J(MAX)}-T_A)/\theta_{JA}$.
Note 3: Measured on JESD51-7, 4-layer PCB.
Note 4: Guaranteed by design.

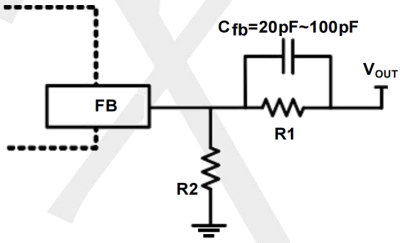
Setting the Output Voltage

The external resistor divider is used to set the output voltage (see Typical Application on page 1). Choose R1 to be around 39kΩ for optimal transient response. R2 is then given by:

Table 1: Selection for Common Output Voltages (VFB=0.765V)

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	C_{FB}(pF)	L (μH)
5	39	7.0	33	4.7
3.3	39	11.7	33	4.7
2.5	39	17.1	33	3.3
1.8	39	28	33	2.2
1.5	39	40	33	2.2
1.2	39	68	33	1.5
1	18	58	33	1.0

$$R_2 = \frac{R_1}{V_{out}/V_{FB} - 1}$$



Feedback Network

Selecting the Inductor

A 1.0μH to 4.7μH inductor with a DC current rating of at least 25% percent higher than the maximum load current is recommended for most applications. For highest efficiency, the inductor DC resistance should be as small as possible. For most designs, the inductance value can be derived from the following equation.

$$L = \frac{V_{out} \times (V_{in} - V_{out})}{V_{in} \times \Delta I_L \times f_{OSC}}$$

Where ΔI_L is the inductor ripple current. Choose inductor ripple current to be approximately 30% if the maximum load current 3A. The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Under light load conditions below 100mA, larger inductance is recommended for improved efficiency.

Selecting the Output Capacitor

The output capacitor (Co1 and Co2) is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right] \times \left[R_{ESR} + \frac{1}{8 \times f_S \times C_2}\right]$$

Where L is the inductor value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor. In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L \times C_2} \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right]$$

In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

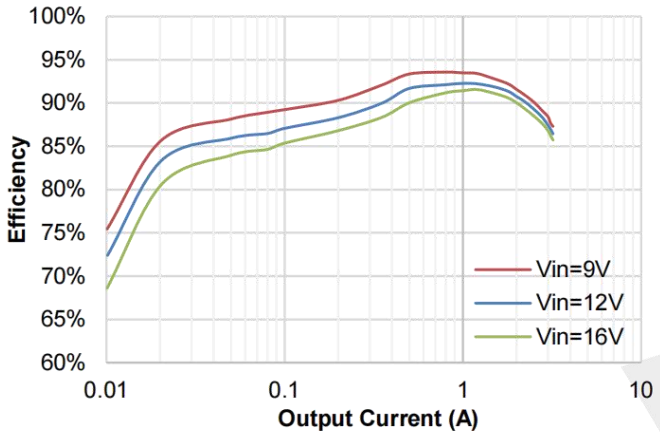
$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right] \times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. The TRWTT3 can be optimized for a wide range of capacitance and ESR values.

Typical Operating Characteristics

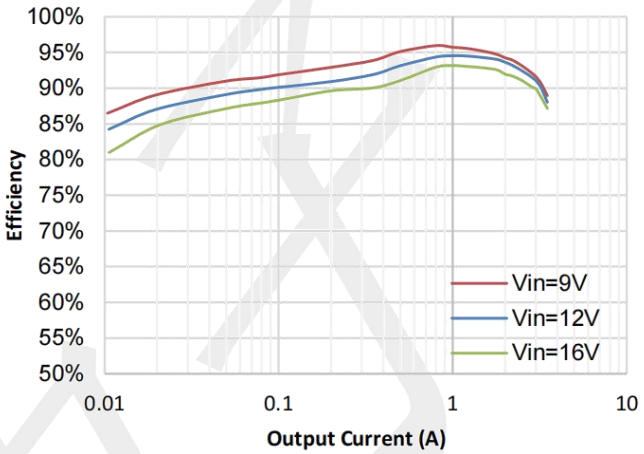
Efficiency

V_{OUT} =3.3V, L=4.7μH, DCR=30mΩ



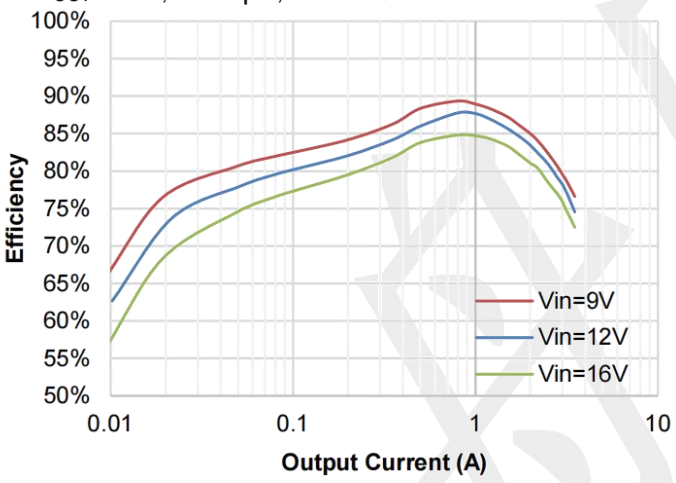
Efficiency

V_{OUT} =5V, L=4.7μH, DCR=30mΩ



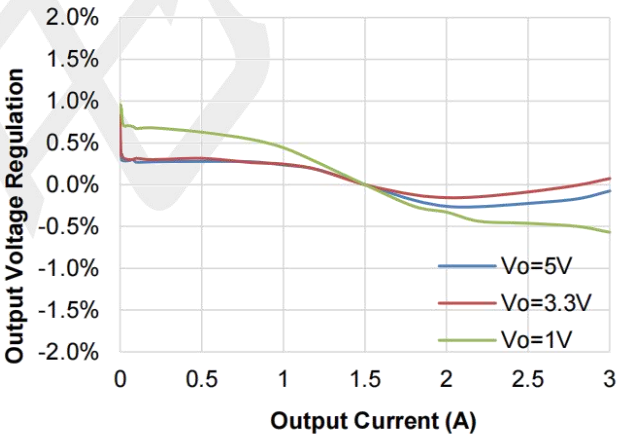
Efficiency

V_{OUT}=1.2V, L=2.2μH, DCR=20mΩ



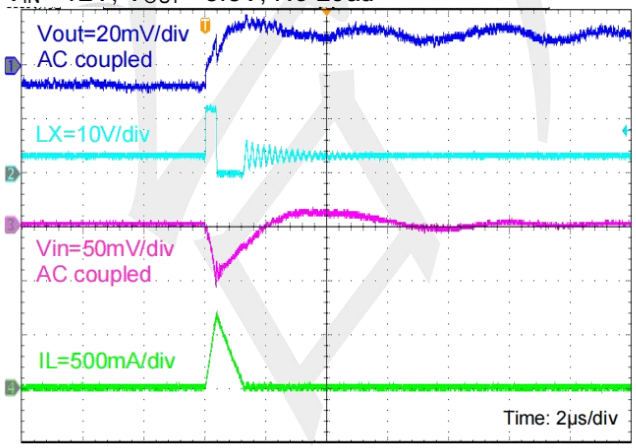
Load Regulation

V_{IN}=12V, T_A=25°C



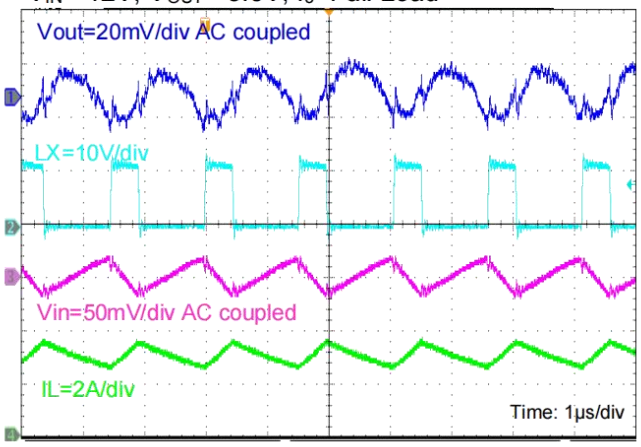
Steady State Operation

V_{IN} =12V, V_{OUT} =3.3V, No Load



Steady State Operation

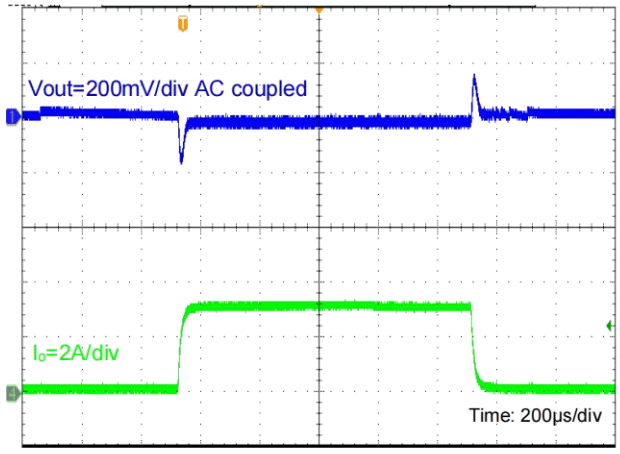
V_{IN} =12V, V_{OUT} =3.3V, I_o=Full Load



Typical Operating Characteristics

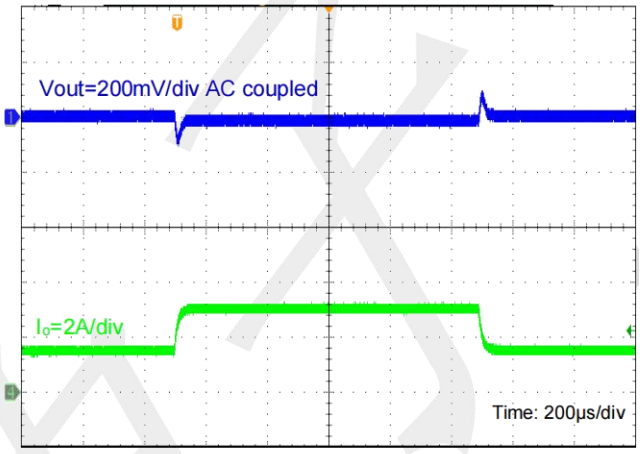
Load Transient

V_{IN} =12V, V_{OUT} =3.3V, I_o =0A to 3A



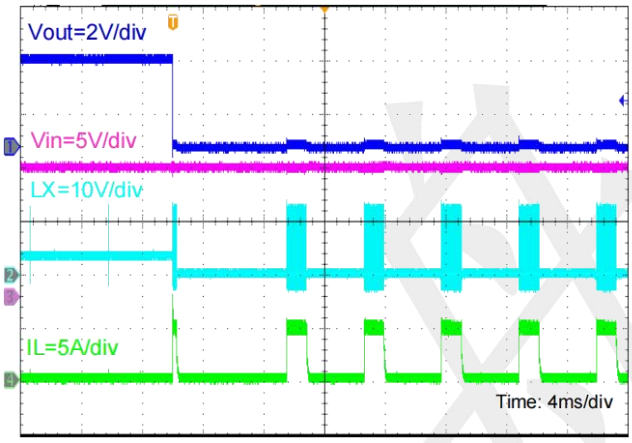
Load Transient

V_{IN} =12V, V_{OUT} =3.3V, I_o =1.5A to 3A



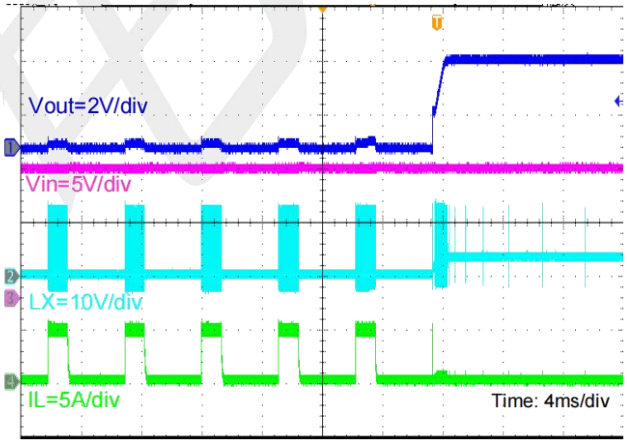
Output Short Entry

V_{IN} =12V, V_{OUT} =3.3V, No Load



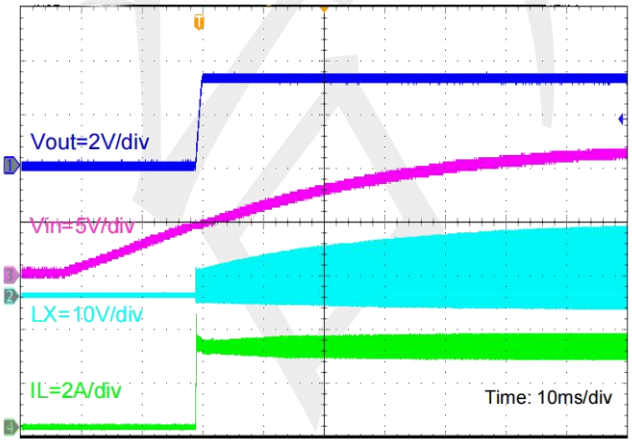
Output Short Recovery

V_{IN}=12V, V_{OUT} =3.3V, No Load



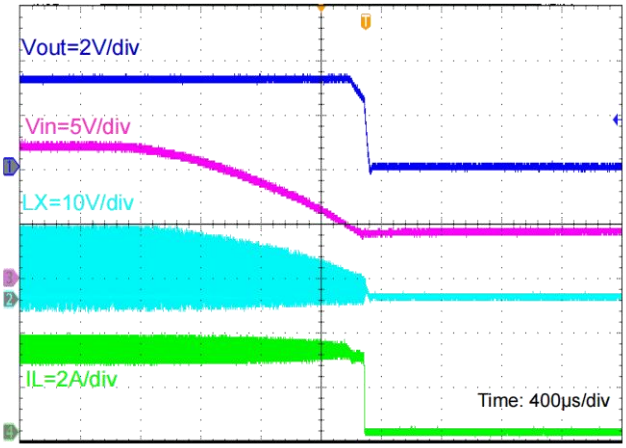
Input Power On

V_{IN} =12V, V_{OUT} =3.3V, I_o =Full Load



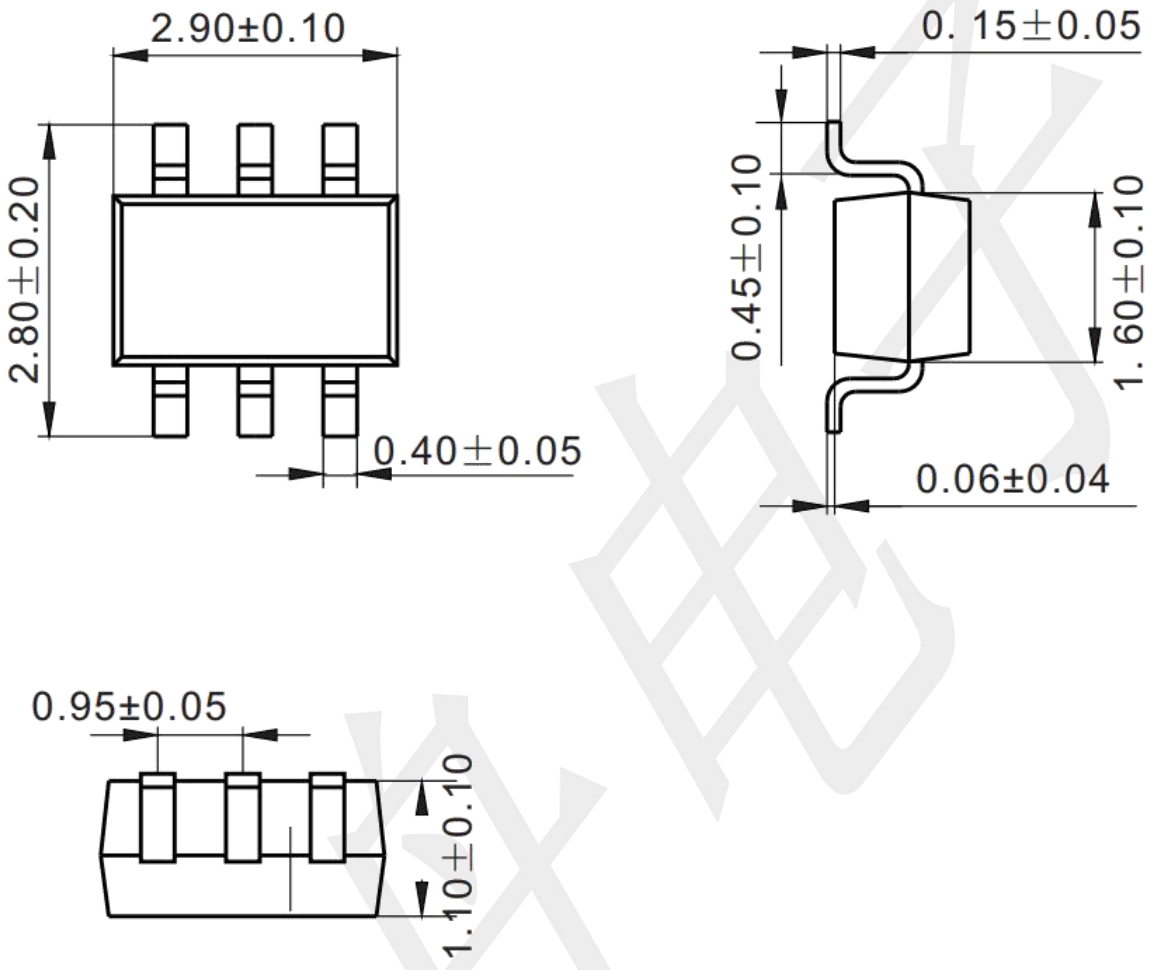
Input Power Down

V_{IN} =12V, V_{OUT} =3.3V, I_o =Full Load



Package Outline Dimensions (unit: mm)

SOT23-6



Mounting Pad Layout (unit: mm)