ULN2803S18

High-current Darlington Transistor Arrays

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Features

- Wide operating voltage range
- Eight-way high-gain Darlington array
- High output voltage (up to 50V)
- High output current (up to 500mA)
- It can be directly connected with TTL, CMOS and PMOS
- Built-in clamp diode for sensitive load

Applications

- Relay drive
- Dc lighting drive
- Stepper motor drive
- Solenoid valve
- Dc brushless motor drive

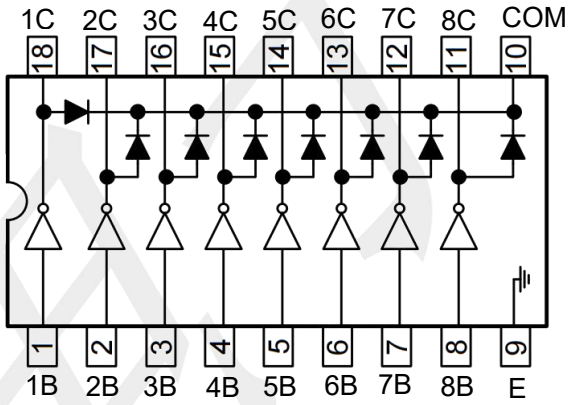
MARKING:



General Description

The are high-voltage, high-current darlington drivers comprised of eight NPN Darlington pairs. All units feature integral clamp diodes for switching inductive loads. Applications include relay, hammer, lamp and display (LED)drivers.

Pinout (top view)



Pin Configurations

Pin Number	Pin Name	Pin Function
1	1B	Input pair1
2	2B	Input pair2
3	3B	Input pair3
4	4B	Input pair4
5	5B	Input pair5
6	6B	Input pair6
7	7B	Input pair7
8	8B	Input pair8
9	E	Common Emitter (ground)
10	COM	Common Clamp Diodes
11	8C	Output pair8
12	7C	Output pair7
13	6C	Output pair6
14	5C	Output pair5
15	4C	Output pair4
16	3C	Output pair3
17	2C	Output pair2
18	1C	Output pair1

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Absolute Maximum Ratings

At 25°C free-air temperature (unless otherwise noted)

Symbol	Parameter		MIN	MAX	UNIT
V_{CC}	Collector to emitter voltage		--	50	**V**
V_R	Clamp diode reverse voltage(2)		--	50	**V**
V_I	Input voltage(2)		--	30	**V**
I_{CP}	Peak collector current	See typical characteristics	--	500	**mA**
I_{OK}	Output clamp current		--	500	**mA**
I_{TE}	Total emitter-terminal current		--	-2.5	**A**
T_A	Operating free-air temperature range		-20	+70	℃
θ_{JA}	Thermal Resistance Junction-to-Ambient(3)		--	63	**°C/W**
θ_{JC}	Thermal Resistance Junction-to-Case(4)		--	12	**°C/W**
TJ	Operating virtual junction temperature		--	+150	℃
T_{STG}	Storage temperature range		-65	+150	℃
ESD	Human Body Modei		--	3000	**V**

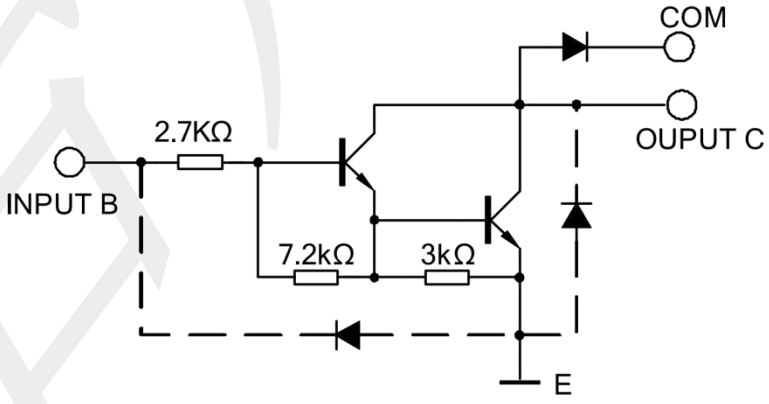
(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated onditions for extended periods may affect device reliability.

(2) All voltage values are with respect to the emitter/substrate terminal E, unless otherwise noted.

(3) Maximum power dissipation is a function of TJ(max), θJA, and TA. The maximum allowable power dissipation at any allowable ambient temperature is PD = (TJ(max) – TA)/θJA. Operating at the absolute maximum TJ of 150°C can affect reliability.

(4) Maximum power dissipation is a function of TJ(max), θJC, and TA. The maximum allowable power dissipation at any allowable ambient temperature is PD = (TJ(max) – TA)/θJC. Operating at the absolute maximum TJ of 150°C can affect reliability

BLOCK DIAGRAM



Note: The input and output parasitic diodes cannot be used as clamp diodes.

Electrical Characteristics

(TA=+25℃, unless otherwise specified)

SYMBOL	PARAMETER	Test Figure	Test Conditions	MIN	TYP	MAX	UNIT
VCC	Collector to Emitter voltage			--	--	50	**V**
TA	Operating Ambient Temperature			-40	--	+105	℃
$V_{I(on)}$	On-state input voltage	Figure 6	VCE = 2 V,IC = 200 mA	--	--	2.4	**V**
			VCE = 2 V,IC = 250 mA	--	--	2.7	**V**
			VCE = 2 V,IC = 300 mA	--	--	3.0	**V**
$V_{CE(sat)}$	Collector-emitter saturation voltage	Figure 5	I_I = 250 μA,IC = 100 mA	--	0.9	1.1	**V**
			I_I = 350 μA,IC = 200 mA	--	1.0	1.3	**V**
			I_I = 500 μA,IC = 350 mA	--	1.2	1.6	**V**
I_{CEX}	Collector cutoff current	Figure 1	VCE = 50 V,I_I = 0	--	--	50	**uA**
		Figure 2	VCE = 50 V,I_I = 0 TA=+150℃	--	--	100	**uA**
V_F	Clamp forward voltage	Figure 8	IF = 350 mA	--	1.7	2.0	**V**
$I_{I(off)}$	Off-state input current	Figure 3	VCE = 50 V, IC = 500 μA	50	65	--	**uA**
I_I	Input current	Figure 4	V_I =3.85V	--	0.93	1.35	**mA**
			V_I =5.0V	--	--	--	**mA**
			V_I =12V	--	--	--	**mA**
I_R	Clamp reverse current	Figure 7	VR = 50 V	--	--	50	**uA**
			VR = 50 V,TA=+70℃	--	--	100	**uA**
Ci	Input capacitance		VI = 0, f = 1 MHz	--	15	25	**PF**

Switching Characteristics

(TA = +25°C, unless otherwise specified)

SYMBOL	PARAMETER	Test Conditions	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	See Figure 9	--	0.25	1.0	**μs**
t_{PHL}	Propagation delay time, high- to low-level output	See Figure 9	--	0.25	1.0	**μs**
V_{OH}	High-level output voltage after switching	VS = 50 V, IO = 300 mA, See Figure 9	VS–20	--	--	**mV**

Parameter Measurement Information

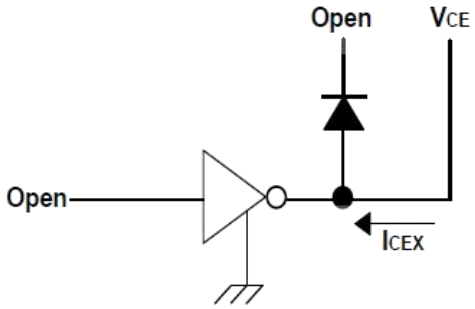


Fig.1 I_{CEX} Test Circuit

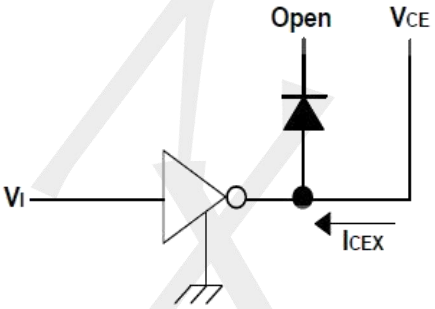


Fig.2 I_{CEX} Test Circuit

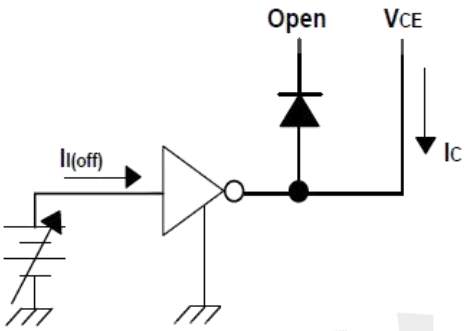


Fig.3 $I_{I(off)}$ Test Circuit

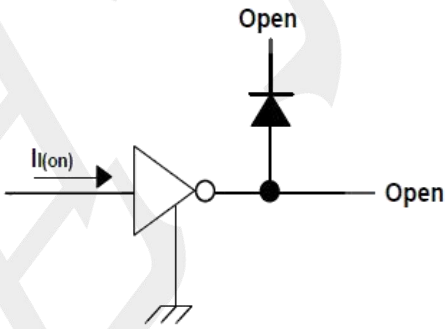


Fig.4 I_I Test Circuit

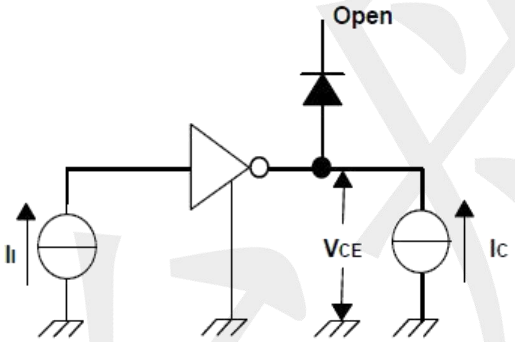


Fig. 5 h_{FE} , $V_{CE(sat)}$ Test Circuit

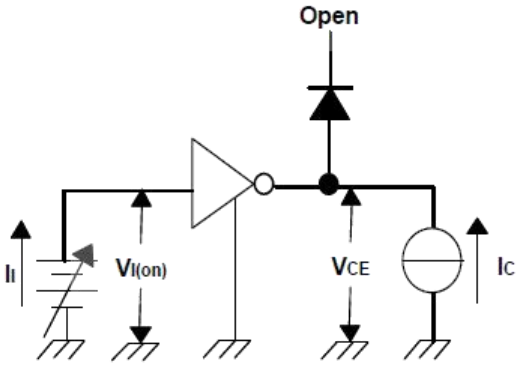


Fig. 6 $V_{I(on)}$ Test Circuit

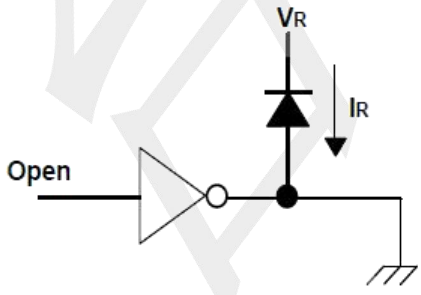


Fig. 7 I_R Test Circuit

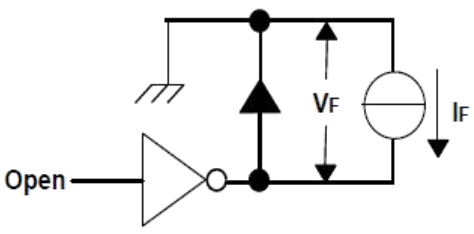


Fig. 8 V_F Test Circuit

Parameter Measurement Information

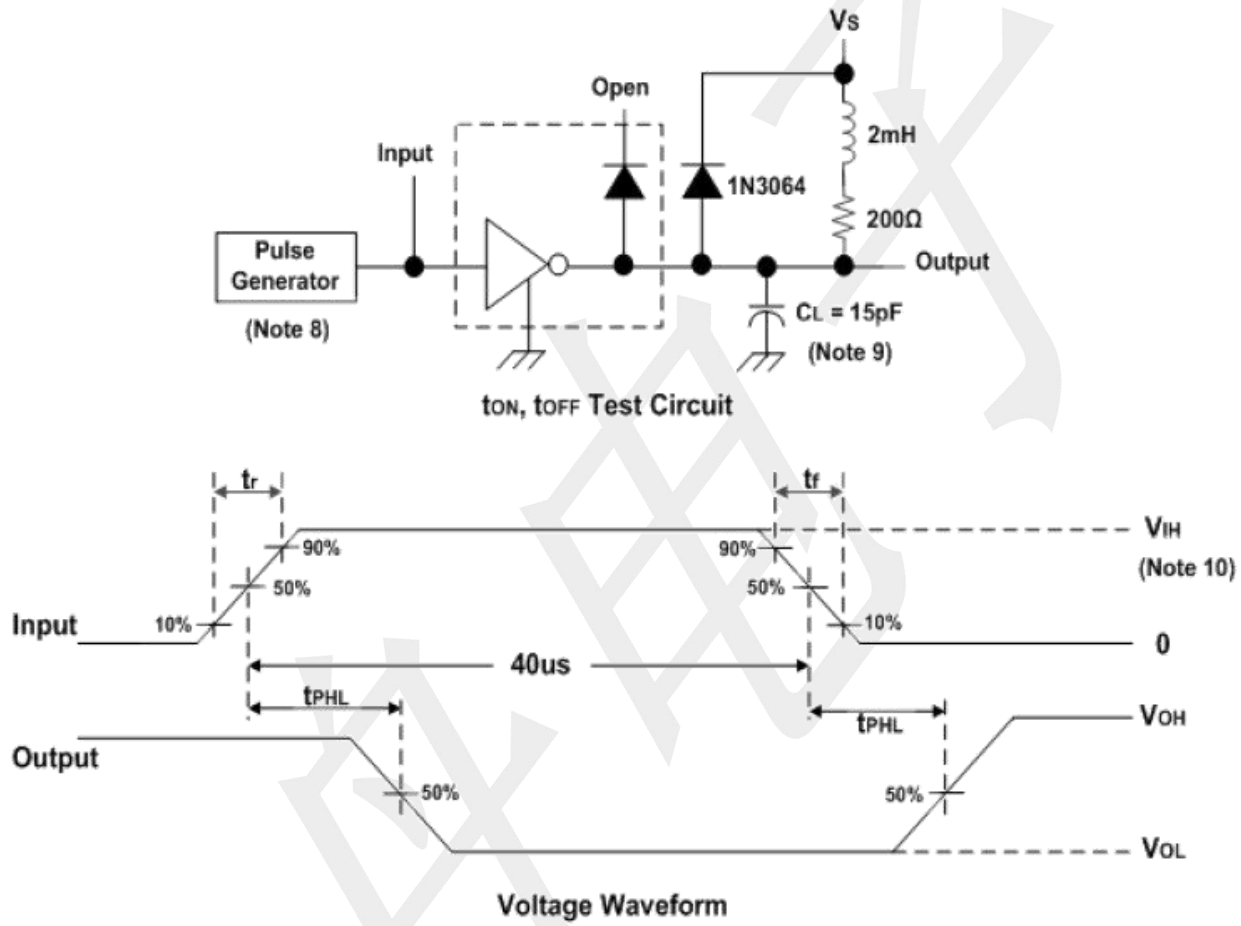
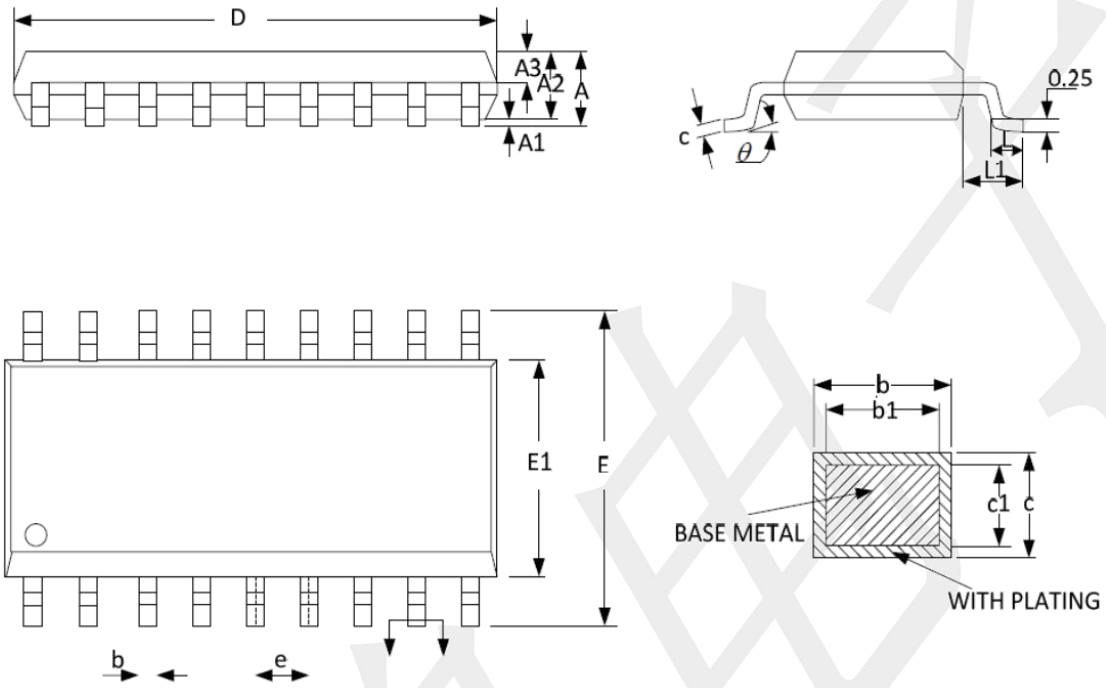


Fig. 9 Latch-Up Test Circuit and Voltage Waveform

Notes: 8. The pulse generator has the following characteristics:
Pulse Width=12.5Hz, output impedance 50Ω, tr≤5ns, tr≤10ns.
9. C_L includes prove and jig capacitance.
10. V_{IH}=3V

Package informantion

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SYMBOL	MILLMETER		
	MIN	NOM	MAX
A	-	-	2.70
A1	0.08	0.18	0.28
A2	2.10	2.30	2.50
A3	0.92	1.02	1.12
b	0.35	-	0.44
b1	0.34	0.37	0.39
c	0.26	-	0.31
c1	0.24	0.25	0.26
D	11.25	11.45	11.65
E	10.10	10.30	10.50
E1	7.30	7.50	7.70
e	1.27BSC		
L	0.70	0.85	1.00
L1	1.40BSC		
θ	0°	-	8°