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TPM30PB30DF8

Dual P-Ch 30V MOSFETS

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Description

The TPM30PB30DF8 is the high cell density trenched P-ch MOSFETs, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications.

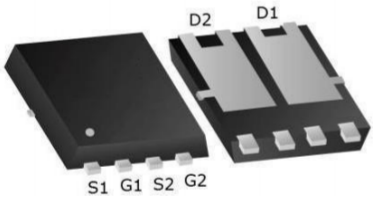
The TPM30PB30DF8 meet the RoHS and Gree Product requirement 100% EAS guaranteed with full function reliability approved.

★ 100% EAS Guaranteed
★ Green Device Available
★ Super Low Gate Charge
★ Excellent CdV/dt effect decline
★ Advanced high cell density Trench technology

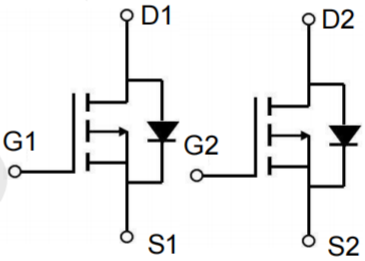
Product Summary

BVDSS	RDSON	ID
-30V	18mΩ	-30A

Pin Configuration



PDFN3333-8L



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	-30	V
V_{GS}	Gate-Source Voltage	±20	V
I_D@T_C=25°C	Continuous Drain Current, V_{GS} @ 10V[1,6]	-30	A
I_D@T_C=100°C	Continuous Drain Current, V_{GS} @ 10V[1,6]	-15.8	A
I_{DM}	Pulsed Drain Current[2]	-100	A
EAS	Single Pulse Avalanche Energy[3]	26.5	mJ
I_{AS}	Avalanche Current	-23	A
P_D@T_C=25°C	Total Power Dissipation[4]	22	W
T_{STG}	Storage Temperature Range	-55 to 150	°C
T_J	Operating Junction Temperature Range	-55 to 150	°C

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient [1]	---	79	°C/W
$R_{\theta JC}$	Thermal Resistance Junction-Case[1]	---	5.7	°C/W

Electrical Characteristics (T_J=25 ℃, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=-250uA	-30	---	---	V
$\Delta BV_{DSS}/\Delta T_J$	BV_{DSS} Temperature Coefficient	Reference to 25℃ , I_D=-1mA	---	---	---	V/℃
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=-10V , I_D=-12A	---	18	23	mΩ
		V_{GS}=-4.5V , I_D=-8A	---	24.5	31	
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS}=V_{DS} , I_D =-250uA	-1	-1.5	-2.5	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	---	---	mV/℃
I_{DSS}	Drain-Source Leakage Current	V_{DS}=-30V , V_{GS}=0V , T_J=25℃	---	---	-1	uA
		V_{DS}=-30, V_{GS}=0V , T_J=100℃	---	---	-5	
I_{GSS}	Gate-Source Leakage Current	V_{GS}=±20V , V_{DS}=0V	---	---	±100	nA
gfs	Forward Transconductance	V_{DS}=-5V , I_D=-10A	---	23.5	---	S
R_g	Gate Resistance	V_{DS}=0V , V_{GS}=0V , f=1MHz	---	---	---	Ω
Q_g	Total Gate Charge	V_{DS}=-15V , V_{GS}=-10V , I_D=-10A	---	20	---	nC
Q_{gs}	Gate-Source Charge		---	3	---	
Q_{gd}	Gate-Drain Charge		---	5.5	---	
$T_{d(on)}$	Turn-On Delay Time	V_{GS}=-10V, V_{DS}=-15V, ID= -10A, R_{GEN}=2.5Ω	---	7.5	---	ns
T_r	Rise Time		---	16	---	
$T_{d(off)}$	Turn-Off Delay Time		---	49	---	
T_f	Fall Time		---	32	---	
C_{iss}	Input Capacitance	V_{DS}=-15V , V_{GS}=0V , f=1MHz	---	980	---	pF
C_{oss}	Output Capacitance		---	137	---	
C_{rss}	Reverse Transfer Capacitance		---	113	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current[1,4]	V_G=V_D=0V , Force Current	---	---	-30	A
V_{SD}	Diode Forward Voltage[2]	V_{GS}=0V , I_S=-30A , T_J=25C	---	---	-1.2	V
t_{rr}	Reverse Recovery Time	IF=-10A ,di/dt=100A / µs , T_J= 2 5 C	---	21	---	nS
Q_{rr}	Reverse Recovery Charge		---	12.5	---	nC

Notes:

1. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150°C
2. The EAS data shows Max. rating . The test condition is DD=-15V, VG=-10V, RG=25ohm, L=0.1mH
3. The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper, The value in any given application depends on the user's specific board design.
4. The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%.
5. This value is guaranteed by design hence it is not included in the production test.

Typical Performance Characteristics

Figure1: Output Characteristics

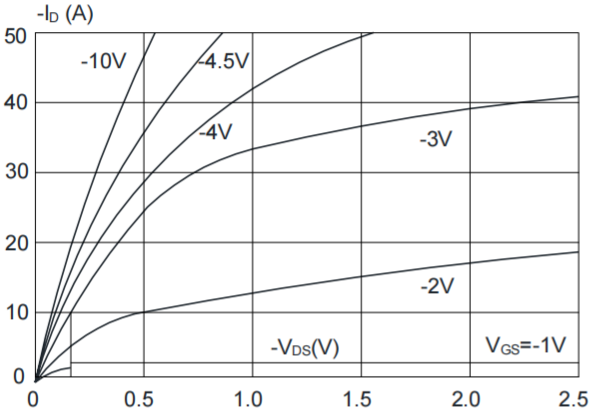


Figure 2: Typical Transfer Characteristics

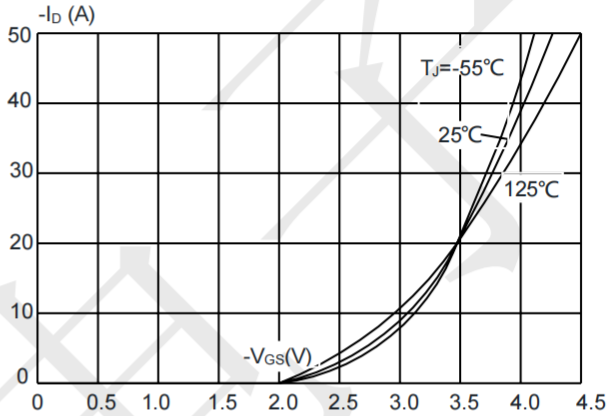


Figure 3: On-resistance vs. Drain Current

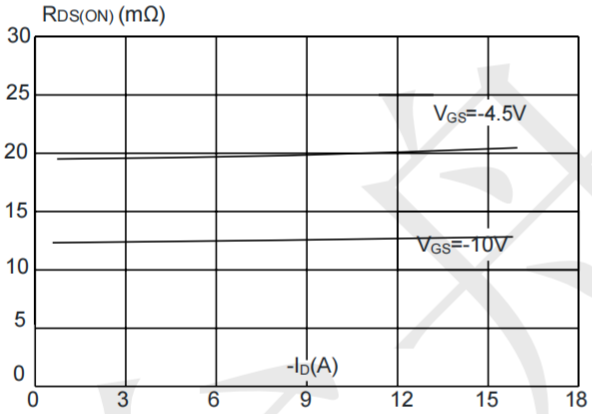


Figure 4: Body Diode Characteristics

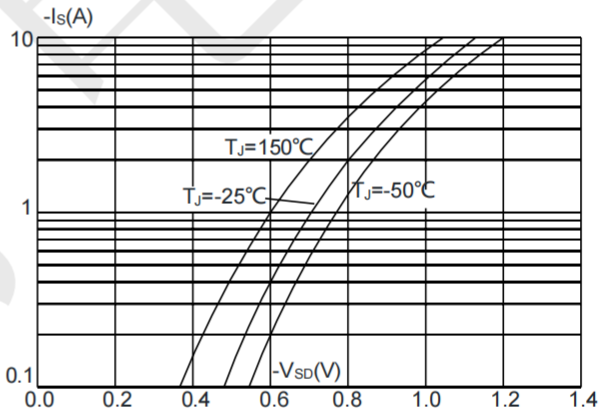


Figure 5: Gate Charge Characteristics

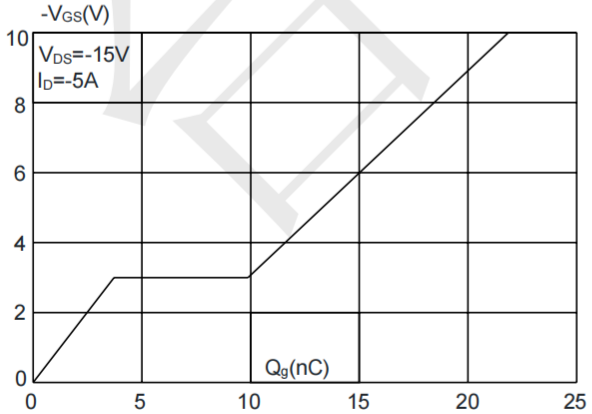
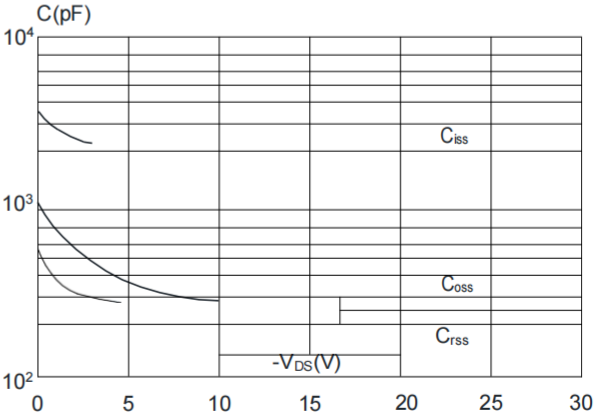


Figure 6: Capacitance Characteristics



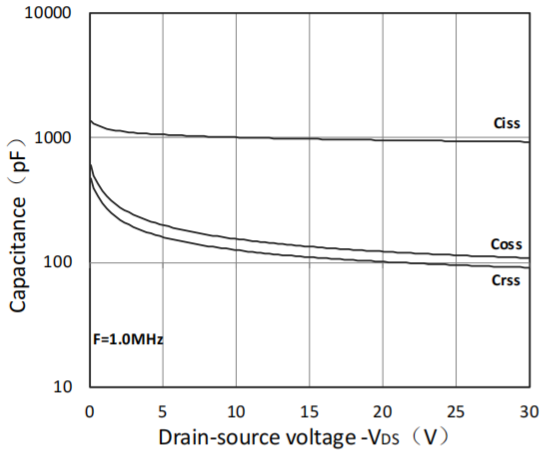


Figure 7. Capacitance Characteristics

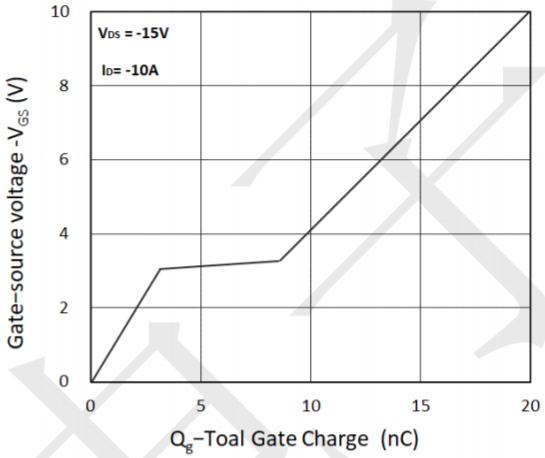


Figure 8. Gate Charge Characteristics

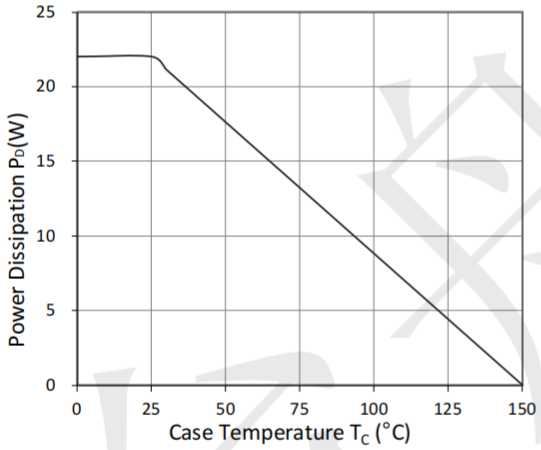


Figure 9. Power Dissipation

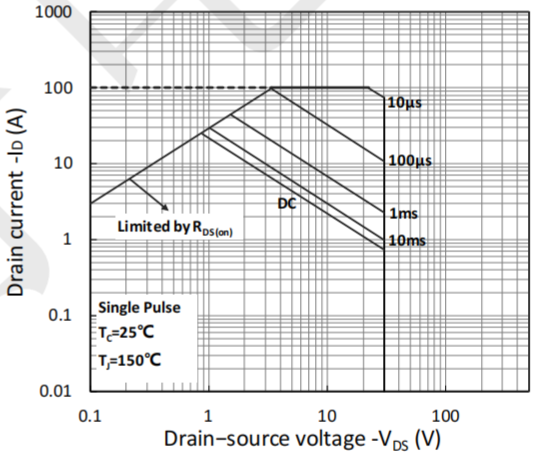


Figure10. Safe Operating Area

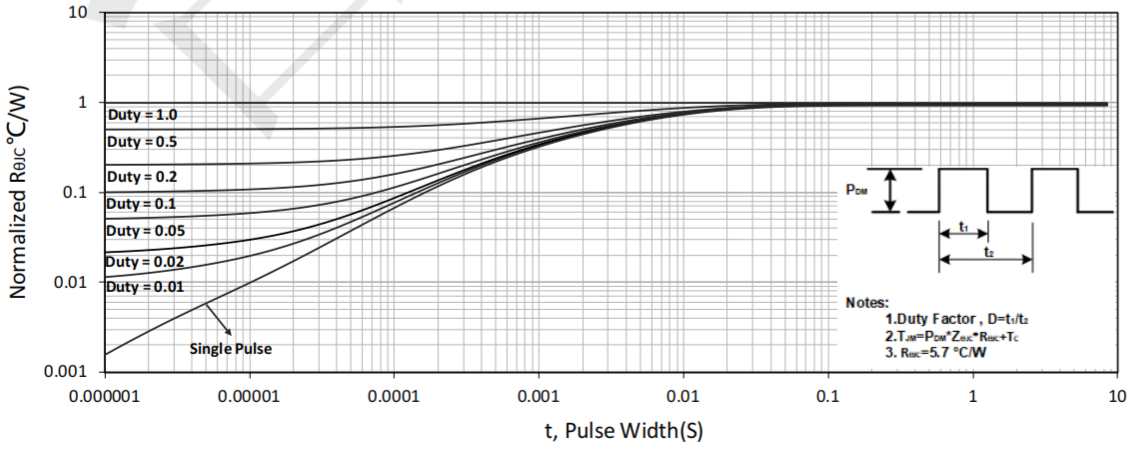
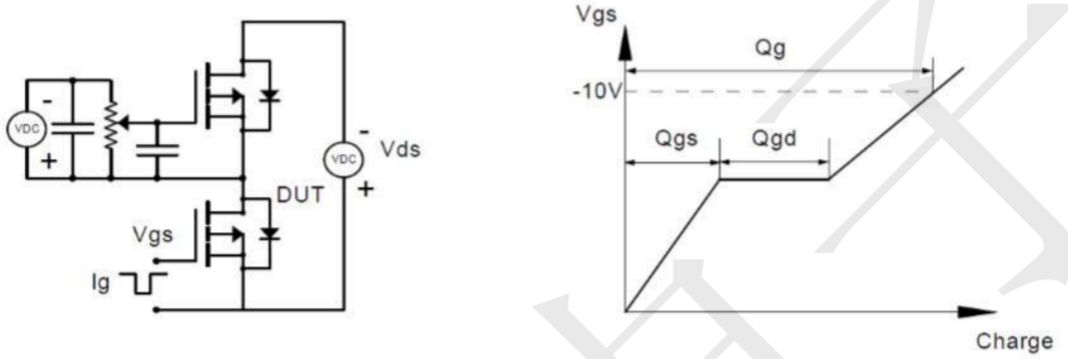


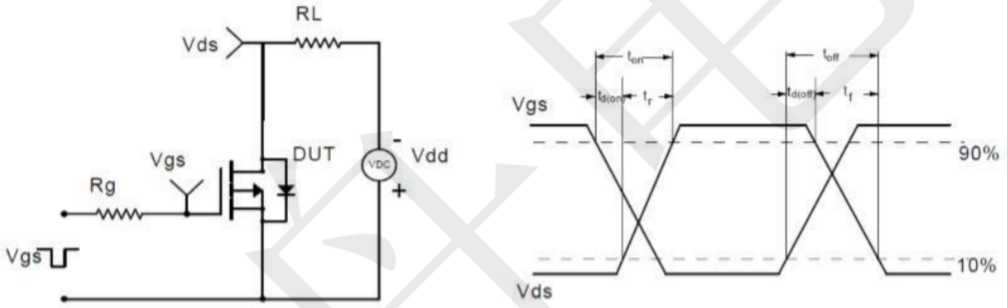
Figure 11. Normalized Maximum Transient Thermal Impedance

Test Circuit

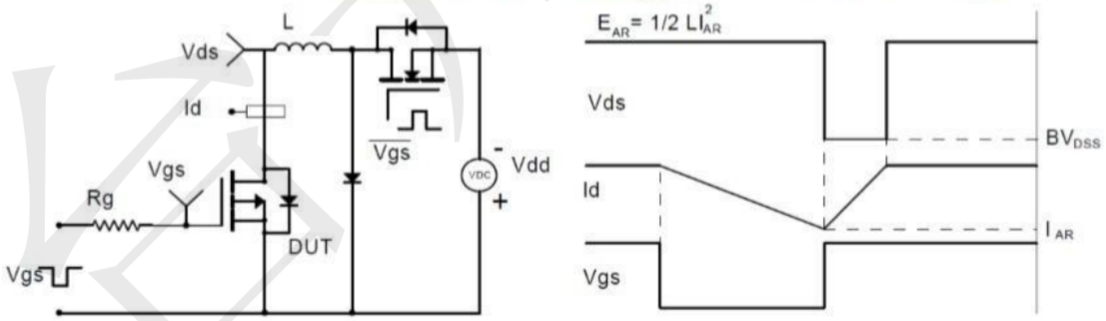
Gate Charge Test Circuit & Waveform



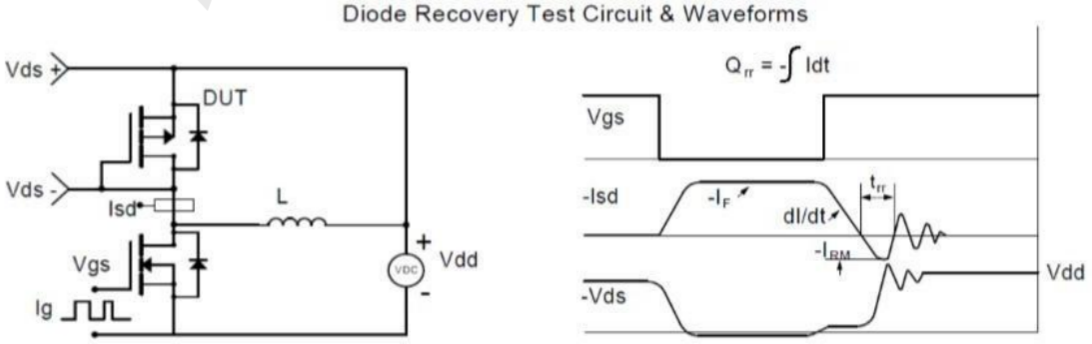
Resistive Switching Test Circuit & Waveforms



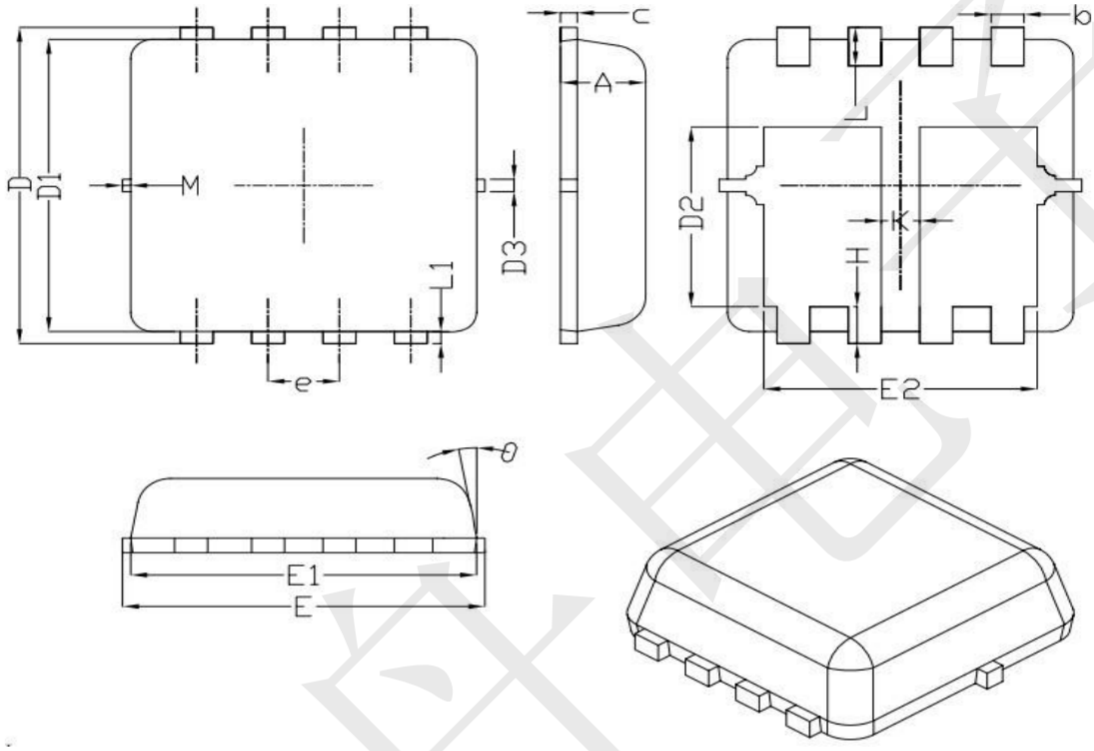
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



Dual PDFN3333-8L Package Outline Data



Symbol	Dimensions (unit: mm)		
	Min	Typ	Max
A	0.70	0.75	0.80
b	0.25	0.30	0.35
c	0.10	0.15	0.25
D	3.25	3.35	3.45
D1	3.00	3.10	3.20
D2	1.78	1.88	1.98
D3	--	0.13	--
E	3.20	3.30	3.40
E1	3.00	3.15	3.20
E2	2.39	2.49	2.59
e	0.65 BSC		
H	0.30	0.39	0.50
L	0.30	0.40	0.50
L1	--	0.13	--
K	0.30	--	--
θ	--	10°	12°
M	*	*	0.15
* Not Specified			

Notes:

1. Refer to JEDEC MO-240 variation CA.
2. Dimensions "D1" and "E1" do NOT include mold flash protrusions or gate burrs.
3. Dimensions "D1" and "E1" include interterminal flash or protrusion.